GEORGIA INSTITUTE OF TECHNOLOGY
OFFICE OF CONTRACT ADMINISTRATION
SPONSORED PROJECT INITIATION

No action
ADS Out

Date: July 15, 1976

Project Title: An Electronics Sports Scoreboard

Project No: A-1851

Project Director: Mr. J. B. Langley

Sponsor: Electro-Mech Corporation; Wrightsville, Georgia 31096

Agreement Period: From May 31, 1976 Until August 31, 1976

Type Agreement: Standard Industrial Research Agreement dated 5/21/76

Amount: $3,546

Reports Required: Final Technical Report

Sponsor Contact Person (s):

Technical Matters	Contractual Matters (thru OCA)
Mr. Charles McMichael President Electro-Mech Corporation Wrightsville, Georgia 31096	Same

Defense Priority Rating: None

Assigned to: Electromagnetics Laboratory (School/Laboratory)

COPIES TO:

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- Division Chief (EES)
- School/Laboratory Director
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- Project Code (GTRI)
- Other _____

CA-3 (3/76)

GEORGIA INSTITUTE OF TECHNOLOGY
OFFICE OF CONTRACT ADMINISTRATION

SPONSORED PROJECT TERMINATION

Date: October 25, 1976

Project Title: An Electronics Sports Scoreboard

Project No: A-1851

Project Director: Mr. J. B. Langley

Sponsor: Electro-Mech Corporation; Wrightsville, Georgia 31096

Effective Termination Date: 10/14/76 (Final Report submitted)

Clearance of Accounting Charges: 10/31/76

Grant/Contract Closeout Actions Remaining:

- x Final Invoice ~~and Closing Documents~~
- _ Final Fiscal Report
- _ Final Report of Inventions
- _ Govt. Property Inventory & Related Certificate
- _ Classified Material Certificate
- _ Other _____

Assigned to: Electromagnetics Laboratory (School/Laboratory)

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Director, Physical Plant
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Project Code (GTRI)
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CA–4 (3/76)

A-1851 Mon RPT 1
16 July 76

ENGINEERING EXPERIMENT STATION
GEORGIA INSTITUTE OF TECHNOLOGY • ATLANTA, GEORGIA 30332

July 13, 1976

Electro-Mech Corporation
Industrial Parkway
Wrightsville, Georgia 31096

Attention: Charles McMicheal

Dear Mr. McMicheal:

Since it has been several weeks since we last talked, I thought I would take some time to bring you up to date on the progress on your micropressor controlled scoreboard project. As you may remember, we are working on two separate problems associated with the scoreboard. One is the microprocessor software(programs) to read the input keyboard, provide the timekeeping functions and generate the appropriate signals to control the lamps in the scoreboard. The second task is to develope an inexpensive method of operating the scoreboard lamps with the microprocessor.

The initial development of the microprocessor software is now complete. The initial development was carried out using the large CDC CYBER 74 computer facility at Georgia Tech to simulate the microprocessor. This has been found to be a much more efficient technique than directly developing programs on the microprocessor. The system which we are presently using employs a relabeled 20 key calculator keyboard. In addition to the 0-9 digit keys, special function keys, labeled H, V, T, P, B, R, S are provided. These indicate to the microprocessor what the numbers entered from the keyboard mean, e.g. Home score, Visitor score, etc. Figure I shows the keyboard in its separate cabinet. The development of the software is now entering its "debugging" phase. The program has been loaded into the actual microprocessor and the remaining minor program errors and such changes as appear necessary will be incorporated in the next several weeks.

Several concepts for driving the display lamps have been investigated. Although it was initially proposed that a multiplex system be used to minimize complexity of the display electronics, more detailed investigation of this approach has uncovered some problems which seem to make this approach unattractive from an economic point of view. Accordingly, we are proceeding with a design which utilizes one driver board per digit. This, we feel, will provide the most economical approach. The design will, at this time, utilize a seven segment numeral forming scheme as is commonly used in calculator displays. It is felt that if a seven segment display is utilized and the electronic components are purchased in production quantities, the driver boards

could be produced for less than $15 per digit. If it is desired to retain the 13 bulb display, it is estimated that a digit driver board could be constructed for approximately $30 per digit.

We are currently planning to have the scoreboard and its controller complete enough to allow a demonstration during the first week in August. If this time period is acceptable to you, we can finalize the exact date as the time approaches. I am sending a copy of this to Bill Craig in hopes that he will be available at that time and also to keep him up to date on this project.

Cordially,

J. B. Langley
Project Director

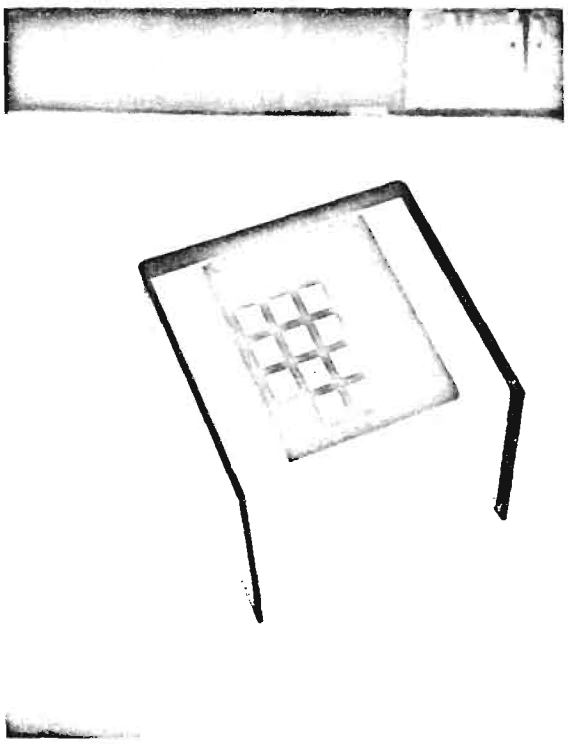

Figure 1. Keyboard

Monthly Rpt. #2
A-1851

ENGINEERING EXPERIMENT STATION
GEORGIA INSTITUTE OF TECHNOLOGY • ATLANTA, GEORGIA 30332

August 11, 1976

Electro-Mech Corporation
Wrightsville, Georgia 31906

Attention: Charles McMicheals

Dear Mr. McMicheals:

I thought I would take a little time to summarize the results of your visit here on 6 August. The microprocessor program development and hardware development portions of the program are now complete as was indicated in the demonstration last Friday. We can easily arrange a further demonstration for you and Mr. Holton at your convenience.

Between now and the end of August, we will complete the documentation of hardware developed and collect data which will allow estimates of costs in production quantities. Also, in the next month a brief study will be made of the best ways to protect the electronics of the scoreboard from possible lightning damage.

If we can provide further assistance, or if you can identify other tasks which you feel are pertinent, please do not hesitate to call me.

Cordially,

John B. Langley

JBL/lcs

A-1851

FINAL REPORT

GIT/EES Project No. A–1851

AN ELECTRONIC SPORTS SCOREBOARD

By

J. B. Langley

Prepared For:

ELECTRO–MECH CORPORATION
WRIGHTSVILLE, GEORGIA 31096

31 August, 1976

1976

ENGINEERING EXPERIMENT STATION
Georgia Institute of Technology
Atlanta, Georgia 30332

FINAL REPORT

AN ELECTRONIC SPORTS SCOREBOARD

Standard Industrial Research Contract

GT/EES Project No. A-1851

Project Director

J. B. Langley

31 August, 1976

for

ELECTRO-MECH Corporation
Wrightsville, Georgia 31096

by

Engineering Experiment Station
Electromagnetics Laboratory
Georgia Institute of Technology
Atlanta, Georgia 30332

FOREWORD

Under a Standard Industrial Agreement arrangement dated May 21, 1976, this project was initiated and conducted in the Electromagnetics Laboratory of the Engineering Experiment Station of the Georgia Institute of Technology under the general supervision of J. W. Dees. The project director was J. B. Langley. Significant contributions to the project were made by C. J. Bowick and D. A. Phillips during the programming and construction of the test elements.

During the program Mr. C. T. McMichael and H. M. Holton of Electro-Mech Corporation visited and observed the elements of the system and the working scoreboard display.

Liason during the program as well as assistance during the initial definition of the task was provided by W. N. Craig, Jr. of the Macon area office as well as R. L. Tessner of the Engineering Experiment Station.

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AN ELECTRONIC SPORTS SCOREBOARD

1.0 INTRODUCTION

During the summer of 1975 a series of discussions were held between personnel of the Macon area office of the Economic Development Laboratory and personnel of the Electro-Mech Corporation. The object of these discussions was the development of an all electronic sports scoreboard to replace the electromechanical (stepping switch) design presently used. The decision to seek a replacement for the existing design was based on both competitive pressures and the recognition that the continuing reduction in the price of integrated circuit electronic components could provide a financially attractive alternate design. Accordingly in the winter of 1976 a meeting was held with representatives of Electro-Mech, E.D.L. and the Electromagnetics Laboratory of the Experiment Station to discuss development of an all electronic sports scoreboard. The eventual outcome of this meeting was Georgia Tech Project A-1851 entitled "An Electronic Sports Scoreboard".

This report describes both the hardware and software (programs) developed under project A-1851 as well as some considerations for protection of an installed system from lightning damage. In addition, estimates of approximate costs to produce the specific circuit elements developed are included.

2.0 TECHNICAL DESCRIPTION

In a microprocessor based device such as the scoreboard it is appropriate to describe the systems in terms of its two major components; the hardware and the software or programs. In general, a design philosophy of maximum use of similar modules is employed in both the hardware and software portions of the scoreboard system. In the hardware portions of the system the philosophy of modularity is primarily manifest in the use of the same circuit for all lamp drivers. In the software the modular concept is implemented through the extensive use of sub-routines in the actual program which controls the scoreboard.

2.1 Hardware

The hardware associated with the electronic sports scoreboard consists of five basic blocks: the keyboard, the microprocessor and line driver, the line receiver and decoder, the digit drivers, and the incandescent lamp displays. Of these, the last three are located physically within the scoreboard itself. These functional

blocks are discussed separately below. Estimated costs to produce these blocks are discussed in Appendix I.

2.1.1. Keyboard

The keyboard employed to furnish data inputs to the microprocessor is a relabeled version of a standard 20 key calculator keyboard. In addition to the digit keys 0-9 additional keys labeled H, V, P, T, B, R, Z, S, and $\frac{C}{CE}$ are included. The lettered keys tell the microprocessor how the numerical data entered by digits 0-9 are to be processed. The functions of the various keys are listed in Table 1. A photograph of the keyboard utilized in the Georgia Tech developed microprocessor controlled scoreboard is shown in Figure 1. For developmental purposes the keyboard was packaged separately from the microprocessor, in a production device. It might be preferable to package the keyboard integrally with the microprocessor.

2.1.2. Microprocessor and Line Driver

A diagram of the microprocessor portion of the system is shown in Figure 2. The design is based on the Motorola MC6800 microprocessor and its associated family of compatible components.

A crystal controlled oscillator is employed to provide the necessary timing information for the microprocessor as well as an accurate one second interval to drive the scoreboard time display. The remaining components are the Random Access Memory (RAM) for short term data storage; the Read Only Memory (ROM) for storage of program; the Parallel Interface Adapter (PIA) for communication with the keyboard; The Asynchronous Communications Interface Adapter (ACIA) used to send the data serially out to the scoreboard and an integrated circuit line driver which provides the power to drive long cables connecting the microprocessor and scoreboard. An addition to the basic keyboard-microprocessor assembly would be a small numeric display similar to the type employed on calculators which would display the data at the scoreboard operators position in addition to the scoreboard

Since the purpose of this project was not the design of a production item, per se, but rather the demonstration of a technique, a Georgia Tech owned microprocessor development system was employed to perform the functions of the device shown in Figure 2. This system, while functionally equivalent to Figure 2, has a slightly different electrical configuration which gives it wider utility in

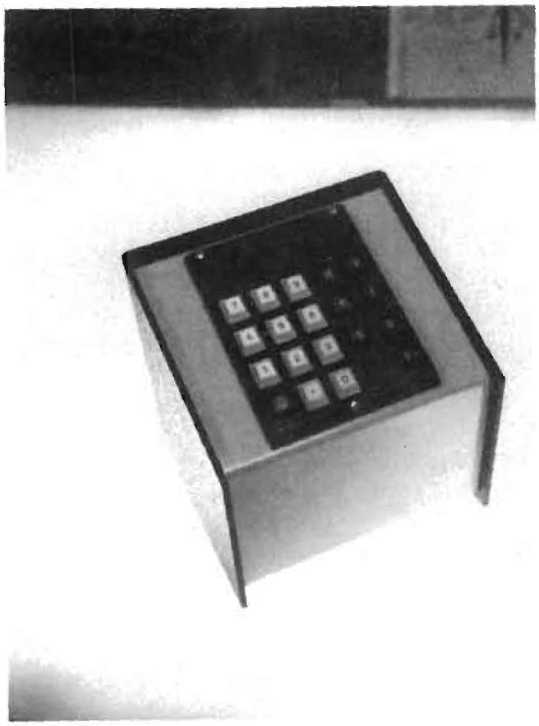


Figure 1. Keyboard.

TABLE 1. KEYBOARD FUNCTIONS

KEY	FUNCTION
H	Home score will be increased by number entered from keyboard
V	As above except Visitor score
P	Sets period light to 1, 2, 3 or 4
T	Sets Time to number entered from keyboard
B	Sets Bonus light
R	Recalls previously entered score or time if entered in error
Z	Sounds buzzer
S	Starts or stops clock
CCE	Clears score or time

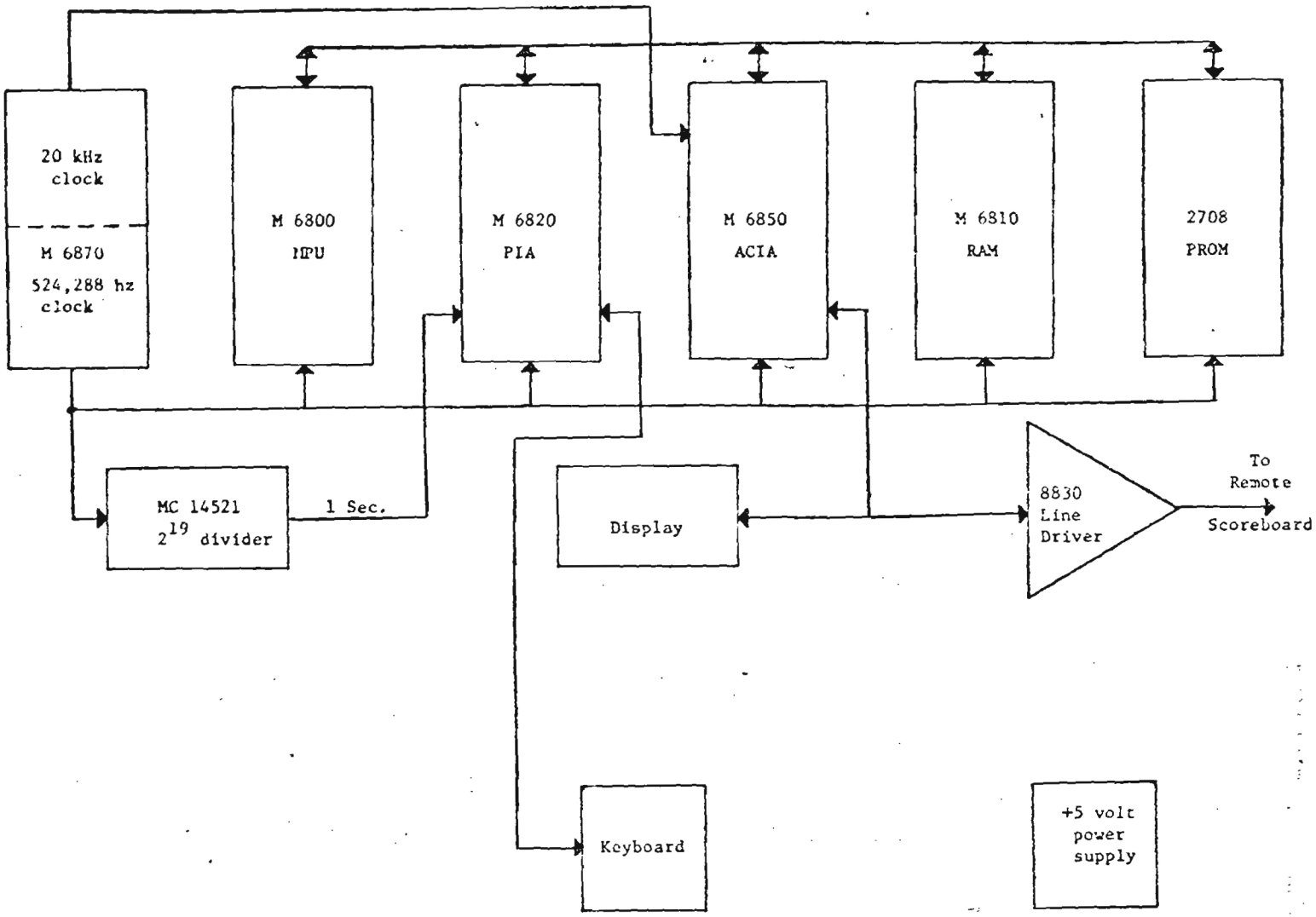


Figure 2. Microprocessor Assembly.

development of microprocessor systems. The principle difference between the system described in Figure 2 and the development system is that in the development system virtually all memory is of the RAM (short term) type which loses its contents on removal of DC power. The primary implication of this is that the program must be reloaded into the microprocessor whenever the machine is turned back on following a power off period. In a production device the program would be permanently stored in a ROM and would remain when power to the system was turned off.

2.1.3 Line Receiver and Decoder

The data transmitted serially by the microprocessor is received at the scoreboard through an integrated circuit line receiver and converted to 8 bit parallel form through the use of a Universal Asynchronous Receiver Transmitter (UART). This integrated circuit with the addition of a timing reference decodes the data sent by the microprocessor and supplies it to the individual digit driver boards. A logic diagram of this circuit is shown in Figure 3. In addition to performing the serial to parallel data conversion, the UART also provides a signal to tell the digit drivers when valid data is available. The engineering model of this circuit has been produced in printed circuit form and is mounted in the scoreboard section supplied to Georgia Tech by Electro-Mech Corporation.

2.1.4 Digit Drivers and Incandescent Lamp Display

The original incandescent lamp digit display developed by Electro-Mech employs 13 bulbs to form the digits 0 through 9. This 13 bulb display has the advantage of forming distinct legible numerals which can be quickly and unambiguously recognized. In the earlier stages of this project it was hoped to be able to retain the 13 bulb display and still provide an economically attractive alternate to the electromechanical stepping switch design. Careful analysis of multiplexing techniques for incandescent lamps revealed that not only would multiplexing be as expensive as providing a separate driver for each digit, but unacceptably short bulb lifetimes would result because of the magnetostrictive loading placed on the filament of each bulb during switching. For this reason the digit driver design employed in the engineering model was chosen. With the advent of the electronic calculator the seven segment display format has gained

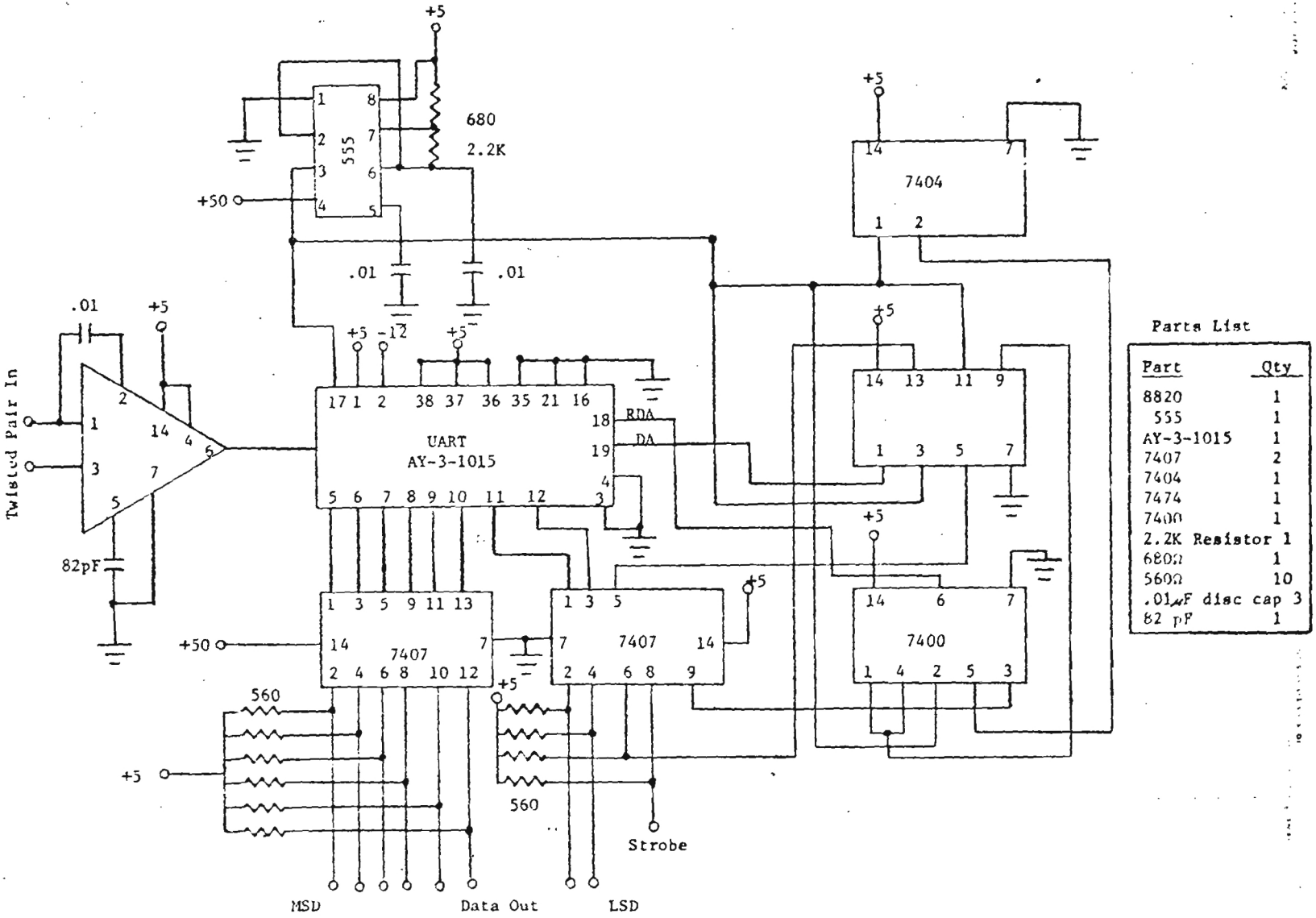


Figure 3. Line Receiver Decoder.

wide acceptance by the general public. An additional result is the ready availability of a wide variety of integrated circuits which perform the conversion of 4 bit binary coded decimal numbers to the seven element coding of the seven segment numeric display. A pseudo-seven segment display was devices for demonstratio purposes by employing elements of the standard Electro-Mech 13 bulb display.

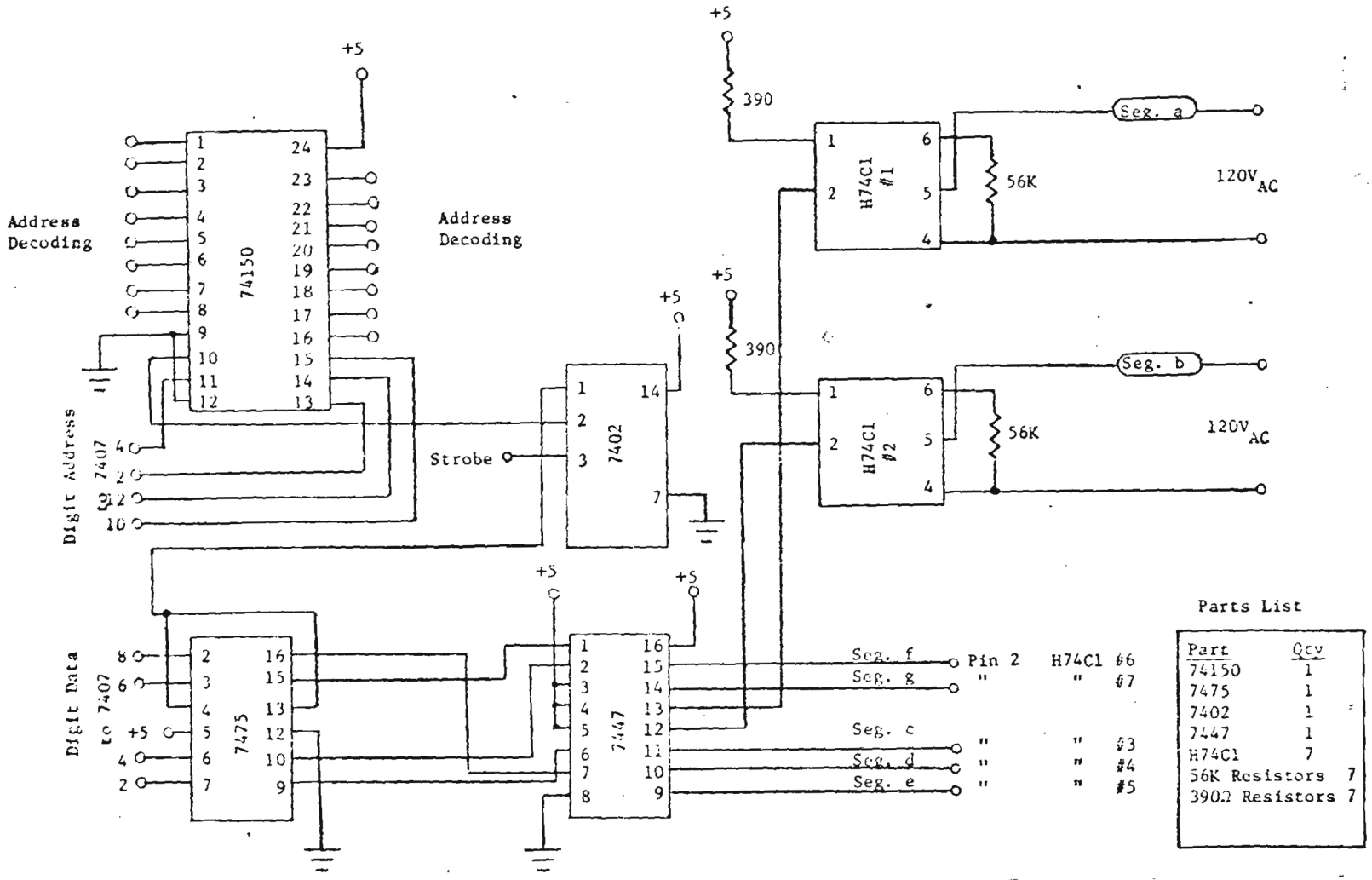
The logic diagram of the digit driver board is shown in Figure 4. The digit driver receives an eight bit data word from the UART consisting of 4 bits of digit data and 4 bits of digit address. Each digit driver board can respond only to one unique address and when that address is received by the appropriate digit driver board the data portion of the 8 bit word is converted to the appropriate signals to drive the seven segments of the display. The data received by each driver is held in a latch so that a flicker free display results. The actual switching of the AC current to the individual lamps is done by optical coupled SCR's which provide total electrical isolation between the AC power lines and low voltage logic control lines in the digit drivers.

2.1.5 Lightning Protection

For electronic equipment which is to be used in an outdoor environment, the possibility of damage due to lightning induced votage transients is always present. Georgia Tech is fortunate in having G. K. Huddleston of the Electrical Engineering School who has had considerable experience in the design and specification of lightning protection equipment for electronic equipment. His recommendations for a cost effective approach to protection of the electronic scoreboard are given in Appendix II.

2.2 Microcomputer Program

The computer program which is stored in the memory of the microcomputer, forms a set of instructions which define the operation of the microprocessor controlled score board. A listing of the actual program is given in Appendix III. This listing is comprised of the actual step by step series of instructions (in mnemonic form), the corresponding machine language instructions and addresses in hexadecimal notation, and a series of comments to explain the program. While a knowledge of the actual programming process for the microprocesser is a requisite for a thorough understanding of the program, the simplified description below will serve to illustrate the essential features of the program written for this application.



Parts List

Part	Qty
74150	1
7475	1
7402	1
7447	1
H74C1	7
56K Resistors	7
390Ω Resistors	7

Figure 4. Digit Driver Board.

An important concept in the creation of a computer program is the idea of a sub-routine. A sub-routine is a small piece of the main program which is used in several places in the main program. By writing the main program as a set of separate sub-routines which are called in sequence by the main program, a modular program is created which can be quite readily modified for different applications. This modification is accomplished by either substituting a new module (sub-routine) for an existing one or adding an additional sub-routine. In addition the various functions of the program are conveniently compacted to minimize the amount of memory space which is required to store the program.

Figure 5 shows a simplified flow chart which illustrates the basic features of the program employed to control the socreboard. When power is applied a start up sub-routine is initiated. This sets several internal functions of the micro-processor to their appropriate states and then starts the main program. The first step of the program is to check the keyboard to see if a key is pressed. If a key is pressed, the program then decides which key is pressed and enters appropriate data into memory. The signal from the one second time interval is also processed and the proper time value is stored in the memory. The program then steps to the output sub-routine which reads the data from the memory, sends it to the ACIA which converts the data to serial from and then transmits it to the scoreboard. The output sub-routine is repeatedly executed until all the data in the memory has been sent. After all data is transmitted (approximately 140 milliseconds) the program then returns to check the keyboard. If no key is pressed, the program jumps directly to the output sub-routine; thus the data is being sent continuously to the scoreboard. This results in an important gain in noise immunity since in the event a burst of noise temporarily causes invalid data to be received at the scoreboard, the correct data will be available within the next 200 millisecond. Thus the noise burst will cause at most a momentary flicker in the data displayed on the scoreboard.

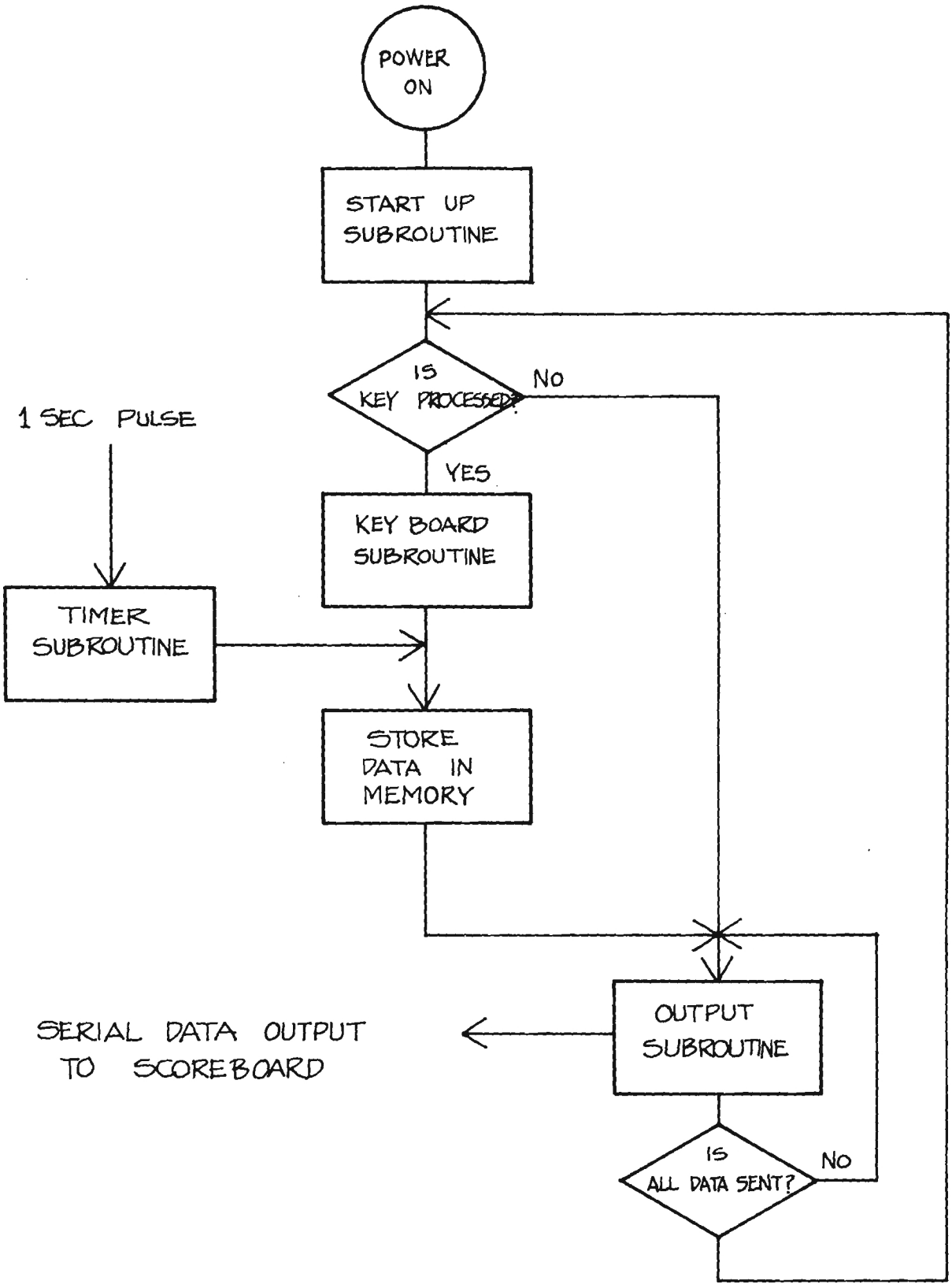


Figure 5. Simplified Flow Chart of Scoreboard Controller.

3.0 Conclusions and Recommendations

It is felt that in terms of the initial objectives of Project A-1851, development of an engineering model of a microprocessor controlled sports scoreboard, the project has been a total success. A working demonstration model has been assembled which employes the essential elements of a workable system. In particular, the circuitry necessary to transmit the data from the microprocessor to the scoreboard and drive a 7 segment incandescent lamp display was developed and produced in printed circuit form. While these printed circuit boards serve to give estimates of the approximate size of final production boards, it would be preferable to lay out new circuit boards for a production system. In laying out new boards, an edge connector could be incorporated into the boards and the size of the boards reduced.

The microcomputer program to operate a basketball scoreboard has been developed. This program will operate the clock, set and increment both home and visitor scores and operate the buzzer either under keyboard control or automatically when the clock reaches zero. In addition, the period lights and bonus lights are also operated from the keyboard. The basic design of the program allows for control of up to sixteen decimal digits on the scoreboard or any combination of decimal digits and control functions totalling sixteen. The changes to the program to expand its scope could be readily implemented through incorporation of new sub-routines.

To bring a microprocessor based electronic sports scoreboard into production, several alternatives are open to the Electro-Mech Corporation:

1) Electro-Mech can subcontract the etching and fabrication of the circuit boards, buy the components and assemble and test the completed system themselves. This option would probably require further design efforts by Georgia Tech to clean up the basic design previously developed, layout final versions of the printed circuit boards and specify components for packaging the production system.
2) Electro-Mech can subcontract the total production of the printed circuit boards and simply plug the boards into appropriate chassis and cabinets which Electro-Mech would wire, and then check out the assembled system. Electro-Mech could either buy the components and

supply them to the subcontractor for assembly or buy totally assembled boards. This approach would also require the engineering services described in 1, above.

3) Electro-Mech could contract to buy some number of complete systems per year from an electronic systems firm. This firm could produce and check out the electronics for both the control unit and the scoreboard unit and supply them in a form suitable for immediate use (or installation) by Electro-Mech. This option would probably also require further engineering services which could possibly be supplied by the vendor and the costs incorporated into their final per-unit price.

Of the three options discussed both 1) and 2) require some considerable internal development by Electro-Mech of the necessary technical skills to fabricate and test a relatively sophisticated electronic system. A significant capital investment in test equipment would be necessary. On a more positive side, these increased capabilities may allow growth into market areas which were not previously open to Electro-Mech products.

The implementation of alternative number 3) would minimize the initial impact of all new scoreboard designs both in terms of the technological support requirement and capital expediture requirement at the expense of the possibility of long term growth. It would seem reasonable that some sort of exclusivity protection could be afforded Electro-Mech in any final agreement with a vendor to supply completed systems.

An optimum course of action for Electro-Mech may be some combination of the three alternatives discussed. For instance, initially it may be desirable to contract for the production of the production of complete systems and later evolve to a point of producing all equipment totally at Electro-Mech. In any event it appears that technical growth at Electro-Mech could be a desirable by-product of a new all electronic scoreboard design.

APPENDIX I

ESTIMATED COSTS

In the following, costs are estimated for each of the three types of circuit developed during this program. The assumptions used in computing these estimates are as follows:

1) Total production: 200 8-digit scoreboards per year
2) Components for all 200 systems purchased in lot
3) Final printed circuit board sizes same as those used in engineering model

Component costs were determined by verbal quotation from Cramer Electronics. Costs for printed circuit board fabrication were supplied by H and L Electronics of Atlanta. Unit costs for printed circuit board operations are given below:

Expose Photoresist and Etch (including stock)	$ 0.15/sq in
Drill holes	0.005/Hole
Solder Plate	0.10/Board
Cut out to finished dimension	0.10/Board

Costs for each of the circuit types are broken down below.

A. Digit Driver Board

The following components would be required:

Item	Qty.	Cost/Item	Total
74150	1600	$ 1.51	2416.00
7475	1600	.49	784.00
7402	1600	.189	302.40
7447	1600	.93	1448.00
H74C1	11,200	1.09	12,208.00
56K Resistors	11,200	.0195	218.40
390Ω Resistors	11,200	.0195	218.40
			$17,635.20

200 8-digit scoreboards would require 1600 digit driver boards. Therefore the projected $17,635.20 total implies a cost per board of $11.02 for components.

The Digit Driver Board cost estimates for printed circuit board fabrication is as follows:

22 sq.in. per PC board @ .15 per sq. in.	$3.30
174 holes @ .005 per hole	.90
.10 per board for solder	.10
.10 per board for cut out	.10
	$4.40 per board

H & L Electronics estimates a cost of $6.00 per board for insertion and wave soldering of components ("stuffing").

The total cost of each board could then be approximated as follows:

Components	$11.02 per board
P.C. Board Fabricated	4.40 per board
P.C. Board "stuffing"	6.00 per board
	$21.42 per board

B. Receiver Board

The following components will be required:

Item	Qty.	Cost/Item	Total
8820	200	$ 4.00	$ 800.00
AY-3-1015	200	7.50	1500.00
555	200	.59	118.00
7407	400	.49	196.00
7404	200	.49	98.00
7474	200	.325	65.00
7400	200	.189	37.80
200Ω	200	.034	6.80
680Ω	200	.953	10.60
560Ω	2000	.021	42.00
.01uF	600	.20	120.00
82pF	200	.20	40.00
			$3034.20

200 8-digit scoreboards would require 200 receiver boards. Therefore the projected $3034.20 total implies a cost per board of $15.17 for components.

The receiver board cost estimate for printed circuit board fabrication is as follows:

22 sq. in. per PC board @ .15 per sq. in.	$3.30
181 holes @ .005 per hole	.91
.10 per board for solder	.10
.10 per board for cut out	.10
	$4.41 per board

The total cost of each board could then be approximated as follows:

Components	$15.17 per board
P.C. Board fabrication	4.41 per board
P.C. Board "stuffing"	6.00 per board
	$25.58 per board

C. Microprocessor and Line Drive Board (including keyboard)

The following components will be required:

Item	Qty.	Cost/Item	Total
M6870	200	$ 36.00	$7200.00
M6800	200	29.95	5990.00
M6820	200	12.00	2400.00
M6850	200	12.00	2400.00
M6810	200	5.00	1000.00
2708	200	65.50*	13100.00*
MC14521	200	7.71	542.00
8830	200	4.00	800.00
Keyboard	200	8.00	1600.00
74C93	200	1.50	300.00
		Total	$35,332.00

This turns out to be $176.66 for each microcomputer system

*Item will only be used in prototype models until a suitable program is developed for the particular scoreboard's application. It's production counterpart in 1000 PC quantities is approximately $15.00

Printed Circuit Costs

48 sq. in. Board @ $ 0.15 sq. in.	$7.20
220 holes @ $ 0.005/hole	1.10
0.10 per board solder	0.10
0.10 per board for cut out	0.10
	$8.50 per board

The total cost of each board can then be estimated as follows:

Components	176.66
P.C. Board fabrication	8.50
P.C. Board "stuffing"	8.00
	$193.16/Board

The total costs per scoreboard, based on the previously stated assumption for the printed circuit board are:

8 digit driver boards @ $21.42	$ 171.36
1 receiver board @ $25.58	25.58
1 microprocessor board	193.16
	$ 390.10

The above price does not reflect packaging cost or power supplies. The cost of packaging is too variable to estimate, however the two power supplies can be estimated to cost less than $60.00 for both.

APPENDIX II

LIGHTNING PROTECTION CONSIDERATIONS

The solid state components used in the scoreboard are susceptible to damage from electrical transients induced on the external electrical wiring by natural lightning and switching on the power system. The transients produced by lightning are much more severe than switching transients; hence, attention is directed to lightning-induced transients and the protection of the circuits from them. Attention is also directed to the permanently installed scoreboard itself.

The points of entry of transients into the scoreboard circuits consist of the twisted pair data transmission line and the 120 Vac power line. The twisted pair is connected to the input terminals of the DM8820A differential line receiver; hence, the DM8820A is susceptible to damage. The 120 Vac power line is connected to the +5 Vdc power supply and to the incandescent lamps and lamp control SCR circuits; hence, these components, especially the SCR's, are susceptible to damage from transients induced on the ac power line.

The transients induced on buried communications cables, such as the twisted pair, can be represented by the worst-case 1000-volt, 10 x 1000 μsec waveform [1]; i.e., a voltage waveform which rises to a peak value of 1000 volts in 10 μsec and decays to half-value in 1000 μsec. (Very little is known about the impedance associated with this voltage waveform.) The voltage is referenced to the metallic shield which surrounds the twisted pair. It is assumed that the shield is tied to earth ground at both ends of the transmission line. Both positive and negative waveforms must be considered.

The pertinent absolute maximum ratings and characteristics of the DM8820A are as follows [2]:

Common-mode voltage	± 20v
Differential-input voltage	± 20v
Inverting input resistance	3.6kΩ (min.)
Non-inverting input resistance	1.8kΩ (min.)

Clearly, some form of protection must be provided to prevent these maximum ratings from being exceeded.

Figure II-1 shows the recommended protection for the input of the DM8820A. Protectors P_1 and P_2 are General Semiconductor Industries, Inc. Type GS1.5K13CA TransZorb™ avalanche diode transient suppressors (bipolar). Resistors R_1 and R_2 are 15-ohm, 2-watt carbon composition resistors which are necessary to limit the peak current through the TransZorbs to less than the 82-ampere rated value (10 x 1000 μsec current waveform) [3]. The TransZorb's have a working voltage of 11.1 volts, breakdown voltage of 12.4-13.7 volts (13 ± 5% volts), and a maximum clamping voltage of 18.2 volts at a peak current of 82 amperes. The response time of the TransZorb clamping action is faster than 10^{-12} seconds as is required for protecting integrated circuits. The TransZorb is available in the standard DO-13 package with 1.25" leads for an approximate cost of $5.00 each in small quantities. The capacitance is less than 0.01 μf and will have no deleterious effect on circuit operation.

Protection P_3 in Figure II-1 is a TII three-electrode gas arrestor type TII-316A [4]. The striking voltage is 150-300 volts (dc). The current rating is 20kA for the standard 8 x 20 μsec waveform and 20A ac for one second. Capacitance is 2 picofarad line to ground. A surge on either line ionizes the rare gas in the common chamber to provide a low impedance path to ground for the surge currents in both lines. The arrestor operates in less than 1 μsec with maximum voltage overshoot of approximately 860 volts for a 10kv/μsec rate of rise and 606 volts overshoot for the 1kv/μsec voltage rate of rise expected from the 10 x 1000 μsec waveform. (The TransZorbs clamp the overshoot to safe values as described above.) After the initial overshoot, the TII arrestor operates in the arc region (characteristic of all gas tubes) and clamps the voltage to the range of 10 to 30 volts [5]. The gas arrestor is a very rugged device and is placed to absorb the brunt of the surges on the twisted pair line. (Note that some impedance is required between the gas arrestor and the TransZorbs in Figure II-1 lest the fast-acting TransZorbs prevent P_3 from "striking".) The TII-316's cost approximately $5.00 each and normally last from 10 to 20 years in moderate lightning environments*.

Figure 2 shows the recommended surge protection for the 120 Vac circuits in the scoreboard which are susceptible to damage from surges entering the system via the 120 Vac power line. Protector P_0 is placed to absorb the brunt of the surges. Protectors P_1 through P_7 may be required to prevent reverse breakdown of the optically coupled SCR's (200 PIV) due to front-of-wave voltages that may get past P_0.

---

*Private communications with John W. Kent, TII.

Protector P_0 is TII-425 power line surge protector which employs a gas tube, thermal circuit breaker, and slow-blow fuse to provide the desired protection [6]. The gas tube used has the same striking characteristics as discussed above for the TII-316. Thermal circuit breakers in each line are required to interrupt the power follow current and quench the arc. A direct in-line slow-blow fuse provides absolute protection against a short circuit. The cost is approximately $27.00.

Protectors P_1 through P_7 in Figure II-2 are bipolar avalanche diode protectors whose breakdown voltage is selected to lie between maximum line voltage (∿170v) and the PIV rating of the SCR's (200v). The resistance of the filaments of the incandescent bulb is used to limit surge currents through the protector. A TransZorb™ GS1.5K200CA is recommended (working voltage V_R = 171 volts, breakdown voltage V_{BD} = 190.0 to 210.0 volts, peak current I_P = 5.5 amperes, 10 x 1000 μsec current waveform). The cost is approximately $5.00 each in small quantities. Other less expensive bipolar avalanche diodes or possibly the General Electric Metal Oxide Varistor ("GE-MOV") type V130LA1 (∿$2.00 each) may be used in Figure II-2 [7]. The use of 400 PIV SCR's is also recommended.

Protection should also be provided for the far end of the transmission line where the DM8830A line driver IC is located. The same arrangement shown in Figure II-1 at the input of the DM8820 should be used on the output of the DM8830. Data sheets for the devices mentioned above are given on pages 18 through 26.

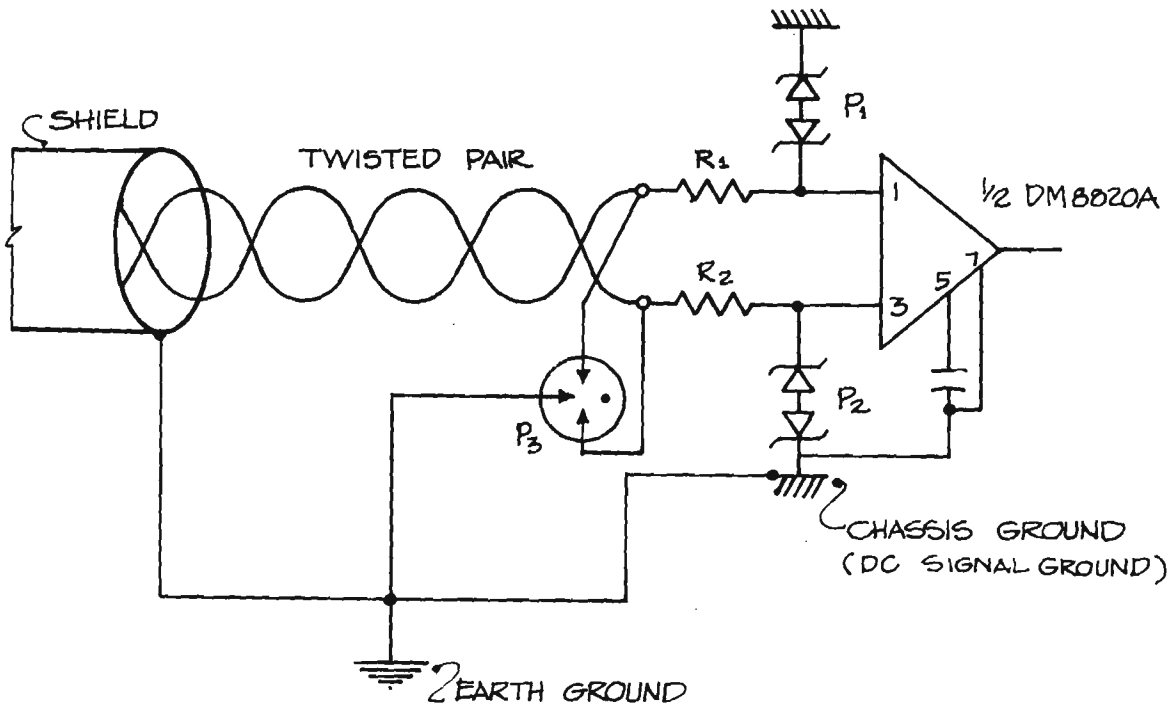


Figure II-1. Recommended Protection for DM8820A Line Receivers.

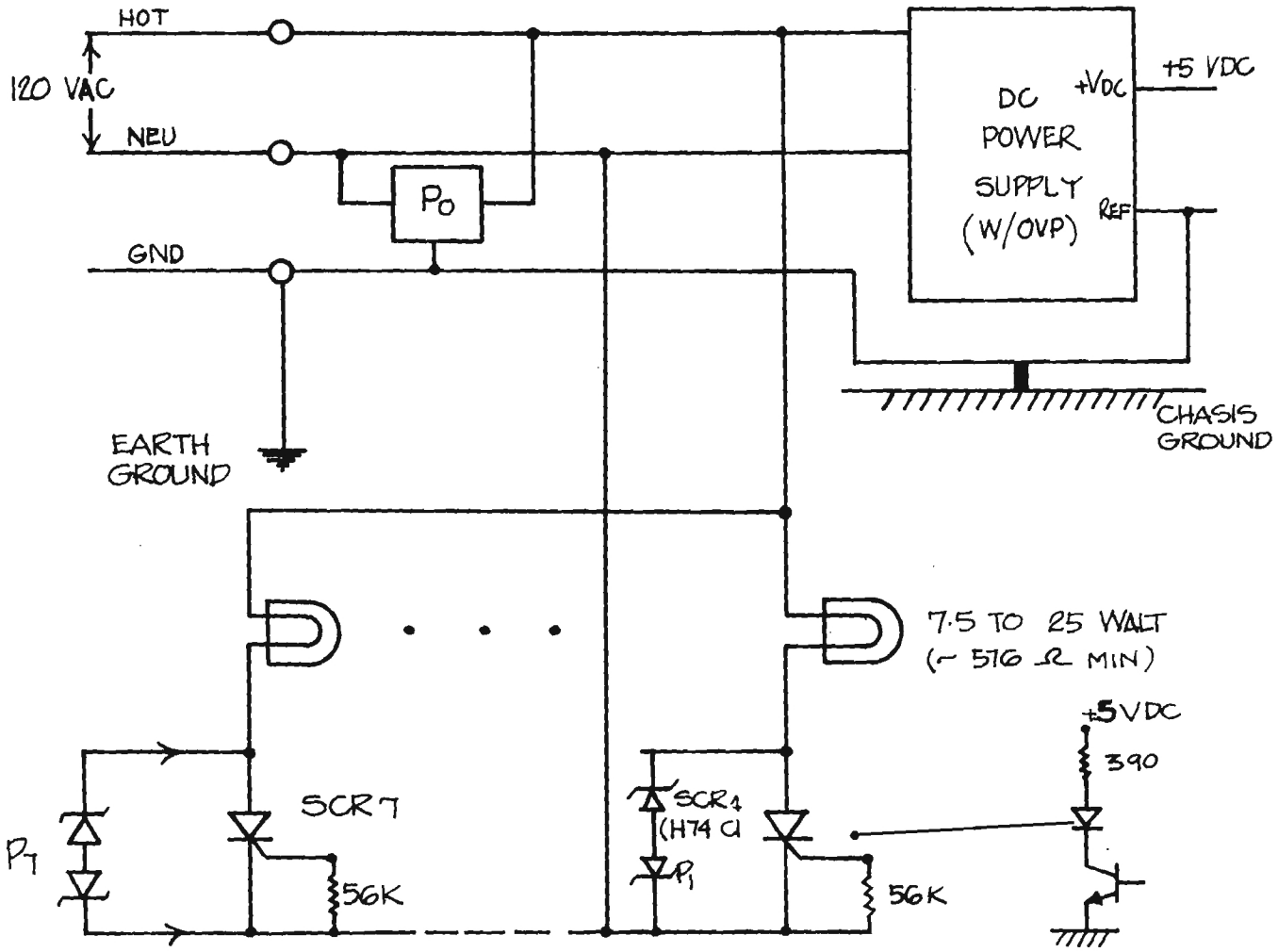


Figure II-2. Recommended Protection for AC Circuits.

APPENDIX II

REFERENCES

1. E. Bennison, A. J. Ghazi, and P. Ferland, "Lightning Surges in Open Wire, Coaxial, and Paired Cables", IEEE Trans, COM-21, No. 10, p. 1136, October 1973.

2. National Semiconductor Corporation, "Interface Integrated Circuits", pp. 4-4 through 4-7, 1974.

3. General Semiconductor Industries, Inc., "TransZorb™ Transient Voltage Suppressors 1N5629 Thru 1N5665A", 2001 West Tenth Place, Tempe, Arizona (Mailing Address: P. O. Box 3078; Telephone 602--968-3101), 1973.

4. Telecommunications Industries, Inc., "3 Electrode Gas Arrestor - TII-316", 1375 Akron Street, Copiague, Long Island, New York, 11726 (Telephone: 842-5000).

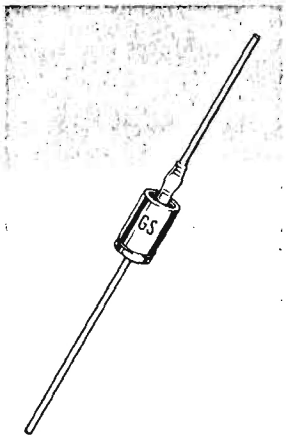
5. C. L. Chen, "FAA Lightning Protection Study: Lightning Protection Devices", Report No. FAA-RD-74-104, Department of Transportation, April 1974.

6. Telecommunications Industries, Inc., "Plug-in Powerline Protector", April 1975.

7. General Electric Company, "Mini-MOV Series", Semiconductor Products Department, Electronics Park, Syracuse, N.Y., 1320, March 1973.

GENERAL SEMICONDUCTOR INDUSTRIES, INC.

TRANSZORB™
TRANSIENT VOLTAGE SUPPRESSORS
1N5629 THRU 1N5665A



DESCRIPTION

This specification sheet defines a series of Silicon Transient Suppressors for use in applications where large voltage transients can permanently damage voltage-sensitive components. The TransZorb is packaged in a hermetically sealed glass-to-metal package and meets all applicable environmental requirements of MIL-S-19500.

The TransZorb has a peak pulse power rating of 1500 watts for 1 millisecond and therefore can be used in applications where induced lightning on rural or remote transmission lines present a hazard to the electronic circuitry. (Reference: R.E.A. Specification P.E. 60). The response time of TransZorb clamping action is effectively instantaneous (better than 1×10^{-12} sec.); therefore, they can protect Integrated Circuits, MOS devices, Hybrids and other voltage-sensitive semiconductors and components. TransZorbs can also be used in series or parallel to increase the peak power ratings.

TransZorbs have proven to be effective in Airborne Avionics and Controls, Mobil Communication Equipment, Computer Power Supplies, Numerically Controlled Machinery, and in many other applications where inductive and switching transients are present.

- **1500 watts peak power dissipation**
- **Available in ranges from 6.8V to 200V.**
- **DO-13 hermetically sealed package**

MAXIMUM RATINGS

- 1500 Watts of Peak Pulse Power dissipation at 25°C (see derating curve)
- $t_{clamping}$ (0 volts to BV min): Less than 1×10^{-12} seconds
- Operating and Storage temperatures: −65° to +175°C
- Forward surge rating: 200 amps, 1/120 second at 25°C
- Steady State power dissipation: 1 watt
- Repetition rate (duty cycle): .01%

MECHANICAL CHARACTERISTICS

- Standard DO-13 package — glass and metal hermetically sealed
- Weight: 1.5 grams (approximate)
- Positive terminal marked with band
- Body marked with GS and type number

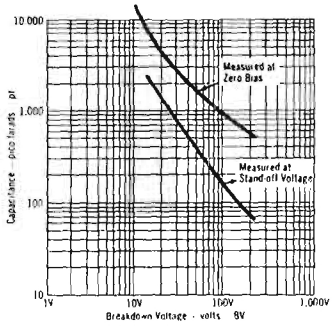
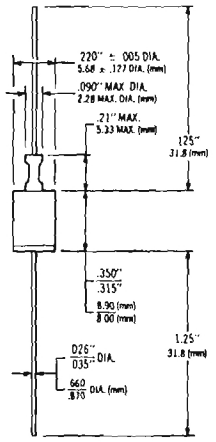


FIGURE 2
Typical Capacitance vs Breakdown Voltage



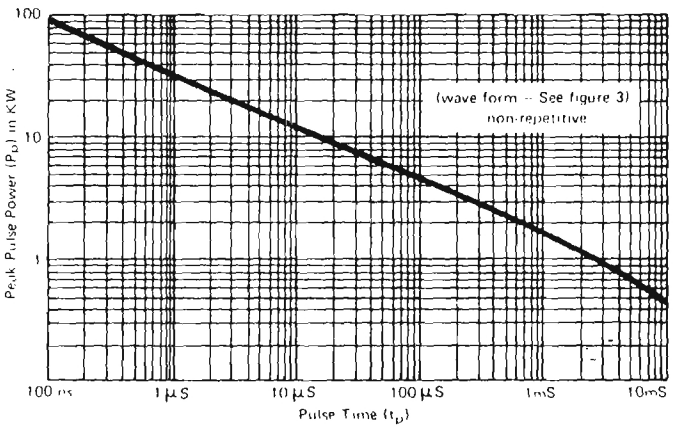


FIGURE 1 — Peak Pulse Power vs Pulse Time

ABBREVIATIONS & SYMBOLS

V_R Stand-Off Voltage. Maximum rated reverse voltage which can be applied to the TransZorb with nonconducting condition. Cathode terminal positive.

I_{PP} Peak Pulse Current

P_P Peak Pulse Power

I_R Reverse Leakage

BV (min) Minimum Breakdown Voltage

V_C (max) Maximum Clamping Voltage. The maximum peak voltage appearing across the TransZorb when subjected to the peak pulse current in a one millisecond time interval. The peak pulse voltages are the combination of voltage rise due to both the internal impedance and thermal rise.

GENERAL SEMICONDUCTOR INDUSTRIES, INC. 2001 West Tenth Place, Tempe, Arizona 85281 • 602-968-3101 • TWX910-950-1942
Mailing Address: P.O. Box 3078

ELECTRICAL CHARACTERISTICS at 25°C

JEDEC TYPE NO.	GS TYPE NO.	Breakdown Voltage BV @ I_T Volts	mA	Reverse Stand-Off Voltage V_R Volts	Maximum Clamping Voltage @ I_{PP} (Fig. 3) V_C Volts	Maximum Reverse Leakage @ V_R I_R μA	Maximum Peak Pulse Current (Fig. 3) I_{PP} A	Maximum Temp. Coef. of BV %/°C
1N5629	1.5K6.8	6.12 - 7.48	10	5.50	10.8	1000	139	.057
1N5629A	1.5K6.8A	6.45 - 7.14	10	5.80	10.5	1000	143	.057
1N5630	1.5K7.5	6.75 - 8.25	10	6.05	11.7	500	128	.061
1N5630A	1.5K7.5A	7.13 - 7.88	10	6.40	11.3	500	132	.061
1N5631	1.5K8.2	7.38 - 9.02	10	6.63	12.5	200	120	.065
1N5631A	1.5K8.2A	7.79 - 8.61	10	7.02	12.1	200	124	.065
1N5632	1.5K9.1	8.19 - 10.0	1	7.37	13.8	50	109	.068
1N5632A	1.5K9.1A	8.65 - 9.55	1	7.78	13.4	50	112	.068
1N5633	1.5K10	9.00 - 11.0	1	8.10	15.0	10	100	.073
1N5633A	1.5K10A	9.5 - 10.5	1	8.55	14.5	10	103	.073
1N5634	1.5K11	9.9 - 12.1	1	8.92	16.2	5	93	.075
1N5634A	1.5K11A	10.5 - 11.6	1	9.40	15.6	5	96	.075
1N5635	1.5K12	10.8 - 13.2	1	9.72	17.3	5	87	.078
1N5635A	1.5K12A	11.4 - 12.6	1	10.2	16.7	5	90	.078
1N5636	1.5K13	11.7 - 14.3	1	10.5	19.0	5	79	.081
1N5636A	1.5K13A	12.4 - 13.7	1	11.1	18.2	5	82	.081
1N5637	1.5K15	13.5 - 16.5	1	12.1	22.0	5	68	.084
1N5637A	1.5K15A	14.3 - 15.8	1	12.8	21.2	5	71	084
1N5638	1.5K16	14.4 - 17.6	1	12.9	23.5	5	64	086
1N5638A	1.5K16A	15.2 - 16.8	1	13.6	22.5	5	67	.086
1N5639	1.5K18	16.2 - 19.8	1	14.5	26.5	5	56.5	.088
1N5639A	1.5K18A	17.1 - 18.9	1	15.3	25.2	5	59.5	.088
1N5640	1.5K20	18.0 - 22.0	1	16.2	29.1	5	51.5	.090
1N5640A	1.5K20A	19.0 - 21.0	1	17.1	27.7	5	54	.090
1N5641	1.5K22	19.8 - 24.2	1	17.8	31.9	5	47	.092
1N5641A	1.5K22A	20.9 - 23.1	1	18.8	30.6	5	49	.092
1N5642	1.5K24	21.6 - 26.4	1	19.4	34.7	5	43	.094
1N5642A	1.5K24A	22.8 - 25.2	1	20.5	33.2	5	45	.094
1N5643	1.5K27	24.3 - 29.7	1	21.8	39.1	5	38.5	.096
1N5643A	1.5K27A	25.7 - 28.4	1	23.1	37.5	5	40	.096
1N5644	1.5K30	27.0 - 33.0	1	24.3	43.5	5	34.5	.097
1N5644A	1.5K30A	28.5 - 31.5	1	25.6	41.4	5	36	097
1N5645	1.5K33	29.7 - 36.3	1	26.8	47.7	5	31.5	.098
1N5645A	1.5K33A	31.4 - 34.7	1	28.2	45.7	5	33	.098
1N5646	1.5K36	32.4 - 39.6	1	29.1	52.0	5	29	.099
1N5646A	1.5K36A	34.2 - 37.8	1	30.8	49.9	5	30	.099
1N5647	1.5K39	35.1 - 42.9	1	31.6	56.4	5	26.5	.100
1N5647A	1.5K39A	37.1 - 41.0	1	33.3	53.9	5	28	.100
1N5648	1.5K43	38.7 - 47.3	1	34.8	61.9	5	24	.101
1N5648A	1.5K43A	40.9 - 45.2	1	36.8	59.3	5	25.3	.101
1N5649	1.5K47	42.3 - 51.7	1	38.1	67.8	5	22.2	.101
1N5649A	1.5K47A	44.7 - 49.4	1	40.2	64.8	5	23.2	.101
1N5650	1.5K51	45.9 - 56.1	1	41.3	73.5	5	20.4	.102
1N5650A	1.5K51A	48.5 - 53.6	1	43.6	70.1	5	21.4	.102
1N5651	1.5K56	50.4 - 61.6	1	45.4	80.5	5	18.6	.103
1N5651A	1.5K56A	53.2 - 58.8	1	47.8	77.0	5	19.5	.103
1N5652	1.5K62	55.8 - 68.2	1	50.2	89.0	5	16.9	.104
1N5652A	1.5K62A	58.9 - 65.1	1	53.0	85.0	5	17.7	.104
1N5653	1.5K68	61.2 - 74.8	1	55.1	98.0	5	15.3	.104
1N5653A	1.5K68A	64.6 - 71.4	1	58.1	92.0	5	16.3	.104
1N5654	1.5K75	67.5 - 82.5	1	60.7	108.0	5	13.9	.105
1N5654A	1.5K75A	71.3 - 78.8	1	64.1	103.0	5	14.6	.105
1N5655	1.5K82	73.8 - 90.2	1	66.4	118.0	5	12.7	.105
1N5655A	1.5K82A	77.9 - 86.1	1	70.1	113.0	5	13.3	.105
1N5656	1.5K91	81.9 -100.0	1	73.7	131.0	5	11.4	.106
1N5656A	1.5K91A	86.5 - 95.5	1	77.8	125.0	5	12.0	.106
1N5657	1.5K100	90.0 -110.0	1	81.0	144.0	5	10.4	.106
1N5657A	1.5K100A	95.0 -105.0	1	85.5	137.0	5	11.0	.106
1N5658	1.5K110	99.0 -121.0	1	89.2	158.0	5	9.5	.107
1N5658A	1.5K110A	105.0 -116.0	1	94.0	152.0	5	9.9	.107
1N5659	1.5K120	108.0 -132.0	1	97.2	173.0	5	8.7	.107
1N5659A	1.5K120A	114.0 -126.0	1	102.0	165.0	5	9.1	.107
1N5660	1.5K130	117.0 -143.0	1	105.0	187.0	5	8.0	.107
1N5660A	1.5K130A	124.0 -137.0	1	111.0	179.0	5	8.4	.107
1N5661	1.5K150	135.0 -165.0	1	121.0	215.0	5	7.0	.108
1N5661A	1.5K150A	143.0 -158.0	1	128.0	207.0	5	7.2	.108
1N5662	1.5K160	144.0 -176.0	1	130.0	230.0	5	6.5	108
1N5662A	1.5K160A	152.0 -168.0	1	136.0	219.0	5	6.8	.108
1N5663	1.5K170	153.0 -187.0	1	138.0	244.0	5	6.2	.108
1N5663A	1.5K170A	162.0 -179.0	1	145.0	234.0	5	6.4	.108
1N5664	1.5K180	162.0 -198.0	1	146.0	258.0	5	5.8	.108
1N5664A	1.5K180A	171.0 -189.0	1	154.0	246.0	5	6.1	.108
1N5665	1.5K200	180.0 -220.0	1	162.0	287.0	5	5.2	.108
1N5665A	1.5K200A	190.0 -210.0	1	171.0	274.0	5	5.5	.108

VF at 100 AMPS PEAK, 8.3 MSEC SINE WAVE equals 3.5 VOLTS MAXIMUM

TransZorbs™ can be used in series or parallel to increase their power handling capability. No precautions are required when using TransZorbs in a series string and power dissipation for two or more devices of the same type is equally shared. When using TransZorbs in parallel it is necessary for the units to be closely matched (approx. .1 volt of each other) in order for equal sharing to take place. Matched sets can be ordered from the factory for a small additional charge.

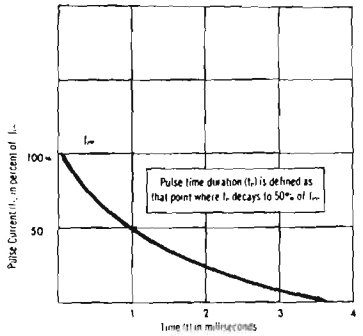


FIGURE 3 — Pulse Wave Form

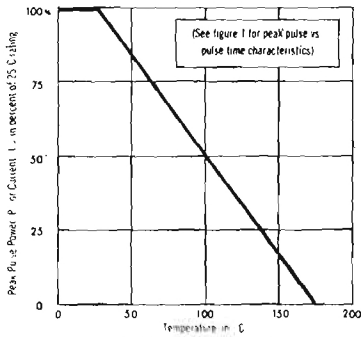


FIGURE 4 — Derating Curve

Non-standard voltage types between those tabulated may be specified as illustrated:

Family Type | Nominal BV | Tolerance Suffix

1.5K 7.2 A

BV Will be Nominal BV ±5% for "A" suffix types and ±10% for non-suffix types at the test current of the next lower standard voltage type.

V_R Will be 85% of Nominal BV for "A" suffix type and 81% of Nominal BV for non-suffix types.

V_C Will be proportionally interpolated between the two neighboring standard types.

I_R Will be that of the next lower standard type.

I_{PP} Will be proportionately interpolated between the two neighboring standard types.

For reverse polarity insert "R" in type number immediately after Nominal BV designation and before the "A" suffix:
Example: 1.5K18RA

BIPOLAR APPLICATIONS

For Bipolar use C or CA Suffix for types 1.5K7.5 through types 1.5K200. Electrical characteristics apply in both directions.

APPENDIX III

PROGRAM LISTING FOR ELECTRONIC SPORTS SCOREBOARD

(Proprietary Information of Electro-Mech Corporation
Wrightsville, Georgia 31096)

MOTOROLA M6800 CROSS ASSEMBLER, RELEASE 1.1

```
00001                           NAM     SCOREBOARD1
00002                       *THIS PROGRAM PARSES A KEYBOARD AND OUTPUTS DATA
00003                       *TO DRIVE AN LED DISPLAY, SIMULATING A BASKETBALL
00004                       *SCOREBOARD.
00005 0000                      ORG     $0000
00006 0000 0001     HOME    RMB     1
00007 0001 0001     VISIT   RMB     1
00008 0002 0001     STATE   RMB     1
00009 0003 0001     DIGIT   RMB     1
00010 0004 0001     FLAG    RMB     1           CLOCK-START FLAG
00011 0005 0001     BUZTIM  RMB     1
00012 0006 0001     LHOME   RMB     1
00013 0007 0001     PERIOD  RMB     1           THIS TABLE MUST BEGIN AT $00C
00014 0008 0002     TIME    RMB     2           BECAUSE OF HOW SWITCHES
00015 000A 0002     SWITCH  RMB     2           ARE CODED.
00016 000C 0167             FDB     SEVEN,EIGHT,NINE,HOMST,VISST,FOUR,FIVE
      000E 0166
      0010 0165
      0012 024B
      0014 0247
      0016 016A
      0018 0169
00017 001A 0166             FDB     SIX,PDINC,CLKSET,ONE,TWO,THREE,BONUS
      001C 022E
      001E 0240
      0020 016D
      0022 016C
      0024 016B
      0026 0163
00018 0028 0162             FDB     RECALL,RESET,BARR,ZERO,BUZZ,CLKCTL
      002A 0164
      002C 01AC
      002E 0160
      0030 023B
      0032 022A
00019 0034 0001     FLAG1   RMB     1           SWITCH-CLOSURE FLAG
00020 0035 0001     FLAG2   RMB     1           SCORE-CLEAR FLAG
00021 0036 0001     LVISIT  RMB     1
00022 0037 0001     BONUSH  RMB     1
00023 0038 0001     BONUSV  RMB     1
00024 0039 0002     POSN    RMB     2
00025 003B 0010     OUT     RMB     16
00026      8008     PIAAD   EQU     $8008
00027      8009     PIAAC   EQU     $8009
00028      800A     PIAED   EQU     $800A
00029      800B     PIAEC   EQU     $800B
00030      8010     ACIAC   EQU     $8010
```

```
00031        8011     ACIAD   EQU     $8011
00032 0048 7F 8009            CLR     PIAAC     SET UP PIAA FOR OUTPUT
00033 004E 73 8008            COM     PIAAD
00034 0051 86 05              LDA A   #$05
00035 0053 B7 8009            STA A   PIAAC
00036 0056 7F 800B            CLR     PIABC     SET UP PIAB FOR INPUT
00037 0059 7F 800A            CLR     PIABD
00038 005C 86 04              LDA A   #$04
00039 005E B7 800B            STA A   PIABC
00040 0061 CE 0000            LDX     #$0000
00041 0064 DF 00              STX     HOME      CLEAR HOME,VISIT
00042 0066 DF 02              STX     STATE     CLEAR STATE,DIGIT
00043 0068 DF 04              STX     FLAG      CLEAR FLAG,BUZTIM
00044 006A DF 34              STX     FLAG1     CLEAR FLAG1,FLAG2
00045 006C DF 37              STX     BONUSH    CLEAR BONUSH,BCNUSV
00046 006E DF 39              STX     POSN      CLEAR POSN
00047 0070 DF 08              STX     TIME      CLEAR TIME
00048 0072 DF 0A              STX     SWITCH    CLEAR SWITCH
00049 0074 86 01              LDA A   #1        SET PERIOD
00050 0076 97 07              STA A   PERIOD
00051 0078 86 13              LDA A   #$13
00052 007A B7 8010            STA A   ACIAC
00053 007D 86 11              LDA A   #$11
00054 007F B7 8010            STA A   ACIAC
00055 0082 CE 0004 START      LDX     #$0004    PARSE KEYBOARD BY LOADING "0"
00056 0085 86 FE              LDA A   #$FE      INTO ONE ROW AND CHECKING THE
00057 0087 0C                 SEC               COLUMNS.  USE INDEX REGISTER
00058 0088 B7 8008 HYU        STA A   PIAAD     TO KEEP TRACK OF THE ROW.
00059 008B F6 800A            LDA B   PIABD
00060 008E 53                 COM B
00061 008F C4 1F              AND B   #$1F
00062 0091 26 0B              BNE     DETB      BRANCH IF SWITCH CLOSURE
00063 0093 09                 DEX
00064 0094 27 03              BEQ     FLGSET
00065 0096 49                 ROL A
00066 0097 20 EE              BRA     HYU
00067 0099 7F 0034 FLGSET     CLR     FLAG1     SET FLAG TO SHOW NO
00068 009C 20 1B              BRA     BUFFER    SWITCH CLOSURES.
00069 009E 96 34    DETB      LDA A   FLAG1     TEST FLAG TO SEE IF
00070 00A0 26 17              BNE     BUFFER    THE SWITCH HAS BEEN
00071 00A2 7C 0034            INC     FLAG1     RELEASED YET.
00072 00A5 4F                 CLR A
00073 00A6 4C       YUU       INC A             DETERMINE ACTIVE COLUMN
00074 00A7 4C                 INC A             ON KEYBOARD.
00075 00A8 54                 LSR B
00076 00A9 26 FA              BNE     YUU
00077 00AB 8B 0A    UFT       ADD A   #$0A      DETERMINE TABLE ADDR FROM
00078 00AD 09                 DEX               WHICH TO GET LOCATION OF
00079 00AE 26 FA              BNE     UFT       SWITCH ROUTINE.
00080 00B0 97 0B              STA A   SWITCH+1
00081 00B2 DE 0A              LDX     SWITCH    X GETS SWITCH CODE.
00082 00B4 EE 00              LDX     X         X GETS ADDRESS OF SWITCH ROUT
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00083 00B6 4F            CLR A
00084 00B7 AC 00         JSR   X          JUMP TO SWITCH ROUTINE
00085 00B9 96 05  BUFFER LDA A BUZTIM     DECREMENT BUZZER TIMER IF SET
00086 00BB 27 03         BEQ   UOC
00087 00BD 7A 0005       DEC   BUZTIM
00088 00C0 5F       UOC  CLR B
00089 00C1 CE 0000       LDX   #$0000
00090 00C4 96 00         LDA A HOME       OUTPUT BUFFER
00091 00C6 8D 6A         BSR   SHIFT
00092 00C8 97 3B         STA A OUT
00093 00CA 96 00         LDA A HOME       DATA IS SHIFTED INTO
00094 00CC 84 F0         AND A #$F0       4 M S BITS OF BYTE.
00095 00CE 26 02         BNE   NOBK1      DATA WORD POSITION IS 4 L S B
00096 00D0 8B 03         ADD A #$03       BLANKS LEADING 0.
00097 00D2 8D 63  NOBK1  BSR   SETUP
00098 00D4 96 01         LDA A VISIT
00099 00D6 8D 5A         BSR   SHIFT
00100 00D8 8D 5D         BSR   SETUP
00101 00DA 96 01         LDA A VISIT
00102 00DC 84 F0         AND A #$F0
00103 00DE 26 02         BNE   NOBK2
00104 00E0 8B 01         ADD A #$01       BLANKS LEADING 0.
00105 00E2 8D 53  NOBK2  BSR   SETUP
00106 00E4 08            INX
00107 00E5 5C            INC B
00108 00E6 96 09         LDA A TIME+1
00109 00E8 8D 48         BSR   SHIFT
00110 00EA 8D 4B         BSR   SETUP
00111 00EC 96 09         LDA A TIME+1
00112 00EE 84 F0         AND A #$F0
00113 00F0 8D 45         BSR   SETUP
00114 00F2 96 08         LDA A TIME
00115 00F4 8D 3C         BSR   SHIFT
00116 00F6 8D 3F         BSR   SETUP
00117 00F8 96 08         LDA A TIME
00118 00FA 84 F0         AND A #$F0
00119 00FC 8D 39         BSR   SETUP
00120 00FE D6 07         LDA B PERIOC
00121 0100 17            TBA
00122 0101 08       PDOUT INX            THIS ROUTINE TURNS ON THE
00123 0102 8D 2E         BSR   SHIFT      CORRECT # OF PERIOC LIGHTS.
00124 0104 8B 04         ADD A #$04
00125 0106 A7 3B         STA A OUT,X
00126 0108 5A            DEC B
00127 0109 26 F5         BNE   PDOUT
00128 010B 96 05  BUZOUT LDA A BUZTIM     TURNS ON THE BUZZER.
00129 010D 27 05         BEQ   BNSOUT
00130 010F 08            INX
00131 0110 86 54         LDA A #$54
00132 0112 A7 3B         STA A OUT,X
00133 0114 96 37  BNSOUT LDA A BONUSH     TURNS ON THE HOME BONUS LIGHT
00134 0116 27 05         BEQ   BNSOT2
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00135 0118 08              INX
00136 0119 86 64           LDA A  #$64
00137 011B A7 38           STA A  OUT,X
00138 011D 96 38    BNSCT2 LDA A  BONUSV   TURNS ON VISITOR BONUS LIGHT.
00139 011F 27 05           BEQ    ERASE
00140 0121 08              INX
00141 0122 86 74           LDA A  #$74
00142 0124 A7 38           STA A  OUT,X
00143 0126 8C 000F ERASE   CPX    #15      FILLS REMAINING OUTPUT BUFFER
00144 0129 27 12           BEQ    OUTPT    LOCATIONS WITH BLANKS./
00145 012B 08              INX
00146 012C 86 04           LDA A  #$04
00147 012E A7 38           STA A  OUT,X
00148 0130 20 F3           BRA    ERASE
00149 0132 48       SHIFT  ASL A
00150 0133 48              ASL A
00151 0134 48              ASL A
00152 0135 48              ASL A
00153 0136 39              RTS
00154 0137 5C       SETUP  INC B
00155 0138 1B              ABA
00156 0139 08              INX
00157 013A A7 38           STA A  OUT,X
00158 013C 39              RTS
00159 013D F6 8010 OUTPT   LDA B  ACIAC   OUTPUT ROUTINE
00160 0140 57              ASR B
00161 0141 57              ASR B          WAIT LOOP FOR ACIA
00162 0142 24 F8           BCC    OUTPT
00163 0144 DE 39           LDX    POSN    NEXT POSITION TO BE OUTPUT.
00164 0146 8C 0004         CPX    #$0004  SKIPS POS. 4 FOR LED DISPLAY.
00165 0149 27 0A           BEQ    REPEAT
00166 014B 8C 0010         CPX    #16
00167 014E 27 0B           BEQ    OVER    DISPLAY FINISHED, BEGIN AGAIN
00168 0150 A6 38           LDA A  OUT,X
00169 0152 B7 8011         STA A  ACIAD   TRANSMIT DATA
00170 0155 7C 003A REPEAT  INC    POSN+1
00171 0158 7E 0082 GO      JMP    START   RETURN TO PARSE KEYBOARD
00172 015B 7F 003A OVER    CLR    POSN+1  WHILE DATA BEING SENT.
00173 015E 20 F7           BRA    GO
00174 0160 88 F4    ZERO   ADD A  #$F4
00175 0162 4C       RECALL INC A
00176 0163 4C       BONUS  INC A
00177 0164 4C       RESET  INC A
00178 0165 4C       NINE   INC A
00179 0166 4C       EIGHT  INC A
00180 0167 4C       SEVEN  INC A
00181 0168 4C       SIX    INC A
00182 0169 4C       FIVE   INC A
00183 016A 4C       FOUR   INC A
00184 016B 4C       THREE  INC A
00185 016C 4C       TWO    INC A
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00186 016D 4C       ONE     INC A


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00187 016E 97 03            STA A  DIGIT
00188 0170 CE 01AC          LDX    #BARB
00189 0173 96 02            LDA A  STATE
00190 0175 27 33    HYY     BEQ    TXY        SUBR LOADS X WITH OFFSET TO
00191 0177 08               INX                GET TO PROPER STATE ROUTINE.
00192 0178 08               INX
00193 0179 4A               DEC A
00194 017A 20 F8            BRA    HYY
00195 017C 7F 0008  TIME4   CLR    TIME
00196 017F 7F 0009          CLR    TIME+1
00197 0182 96 03            LDA A  DIGIT      SUBR TO PRESET CLOCK.
00198 0184 8D AB            BSR    SHIFT
00199 0186 97 08            STA A  TIME       LOAD DIGIT INTO MS BITS
00200 0188 7A 0002          DEC    STATE      OF WORD 1 OF TIME.
00201 018B 39               RTS
00202 018C 96 03    TIME3   LDA A  DIGIT
00203 018E 9B 08            ADD A  TIME       LOAD NEXT DIGIT INTO LS BITS
00204 0190 97 08            STA A  TIME       OF WORD 1 OF TIME.
00205 0192 7A 0002          DEC    STATE
00206 0195 39               RTS
00207 0196 96 03    TIME2   LDA A  DIGIT      LOAD THIRD DIGIT INTO MS BITS
00208 0198 8D 97            BSR    SHIFT
00209 019A 97 09            STA A  TIME+1
00210 019C 7A 0002          DEC    STATE
00211 019F 39               RTS
00212 01A0 96 03    TIME1   LDA A  DIGIT      LOAD LAST DIGIT INTO LS BITS
00213 01A2 9B 09            ADD A  TIME+1     OF WORD 2 OF TIME.
00214 01A4 97 09            STA A  TIME+1
00215 01A6 7A 0002          DEC    STATE
00216 01A9 39               RTS
00217 01AA 6E 00    TXY     JMP    X          JUMP TO PROPER STATE ROUTINE.
00218 01AC 39       BARB    RTS
00219 01AD 02               NOP
00220 01AE 20 EF            BRA    TIME1
00221 01B0 20 E3            BRA    TIME2
00222 01B2 20 D7            BRA    TIME3
00223 01B4 20 C5            BRA    TIME4
00224 01B6 20 35            BRA    VDIG
00225 01B8 D6 03    HDIG    LDA B  DIGIT      INCREMENT HOME SCORE.
00226 01BA C1 0B            CMP B  #11
00227 01BC 27 56            BEQ    HBON       BRANCH IF BONUS WAS PUSHED.
00228 01BE 2E 28            BGT    RCLH       BRANCH IF RECALL WAS PUSHED.
00229 01C0 96 00            LDA A  HOME       SAVE PREVIOUS SCORE.
00230 01C2 97 06            STA A  LHOME
00231 01C4 C1 0A            CMP B  #10
00232 01C6 2C 07            BLT    HOME1      BRANCH TO ADDITION ROUTINE.
00233 01C8 7C 0035          INC    FLAG2      SET FLAG -- 2 DIGITS NEEDED
00234 01CB 7F 0000          CLR    HOME       BECAUSE CLEAR WAS PUSHED.
00235 01CE 39               RTS                CLEAR HOME SCORE.
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00236 01CF 96 35    HOME1   LDA A   FLAG2
00237 01D1 27 0C            BEQ     HONE        BRANCH TO SINGLE DIGIT ADDN.
00238 01D3 4F               CLR A
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00239 01D4 97 35            STA A   FLAG2
00240 01D6 5D       RITA    TST B               SUBR ADDS PROPER # OF 10'S
00241 01D7 27 0C            BEQ     DONE        TO HOME SCORE.
00242 01D9 8B 0A            ADD A   #10
00243 01DB 19               DAA
00244 01DC 5A               DEC B
00245 01DD 20 F6            BRA     RITA
00246 01DF 97 02    HONE    STA A   STATE       CLEAR STATE
00247 01E1 17               TBA                 ADDS DIGIT TO HOME SCORE.
00248 01E2 9B 00            ADD A   HOME
00249 01E4 19               DAA
00250 01E5 97 00    DONE    STA A   HOME
00251 01E7 39               RTS
00252 01E8 96 06    RCLH    LDA A   LHOME
00253 01EA 97 00            STA A   HOME        HOME GETS PREVIOUS SCORE.
00254 01EC 39               RTS
00255 01ED 96 03    VDIG    LDA B   DIGIT       INCREMENT VISITOR'S SCORE.
00256 01EF C1 0B            CMP B   #11
00257 01F1 27 33            BEQ     VBON        BRANCH IF BONUS WAS PUSHED.
00258 01F3 2E 2C            BGT     RCLV        BRANCH IF RECALL WAS PUSHED.
00259 01F5 96 01            LDA A   VISIT       SAVE PREVIOUS SCORE.
00260 01F7 97 36            STA A   LVISIT
00261 01F9 C1 0A            CMP B   #10
00262 01FB 2C 07            BLT     VISIT1      BRANCH TO ADDITION ROUTINE.
00263 01FD 7C 0035          INC     FLAG2       SET FLAG -- 2 DIGITS NEEDED
00264 0200 7F 0001          CLR     VISIT       BECAUSE CLEAR WAS PUSHED.
00265 0203 39               RTS                 CLEAR VISIT SCORE.
00266 0204 96 35    VISIT1  LDA A   FLAG2
00267 0206 27 10            BEQ     VONE        BRANCH TO SINGLE DIGIT ADDN.
00268 0208 4F               CLR A
00269 0209 97 35            STA A   FLAG2
00270 020B 5D       RITA1   TST B               SUBR ADDS PROPER # OF 10'S
00271 020C 27 10            BEQ     DONE1       TO VISTIOR SCORE.
00272 020E 8B 0A            ADD A   #10
00273 0210 19               DAA
00274 0211 5A               DEC B
00275 0212 20 F6            BRA     RITA1
00276 0214 73 0037  HBON    COM     BONUSH      SET-RESET BONUS FLAG.
00277 0217 39               RTS
00278 0218 97 02    VONE    STA A   STATE       CLEAR STATE
00279 021A 17               TBA                 ADDS DIGIT TO VISIT SCORE.
00280 021B 9B 01            ADD A   VISIT
00281 021D 19               DAA
00282 021E 97 01    DONE1   STA A   VISIT
00283 0220 39               RTS
00284 0221 96 36    RCLV    LDA A   LVISIT
00285 0223 97 01            STA A   VISIT       VISIT GETS PREVIOUS SCORE./
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00286 0225 39                RTS
00287 0226 73 0059 VBON      COM     BONUSV    SET-RESET BONUS FLAG.
00288 0229 39                RTS
00289 022A 73 0004 CLKCTL    COM     FLAG      START-STOP CLOCK CONTROL.
00290 022C 39                RTS
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00291 022E 96 07   PCINC   LDA A   PERIOD    INCREMENT PERIOD.
00292 0230 80 03           SUB A   #3
00293 0232 2E 04           BGT     WHEN
00294 0234 7C 0007         INC     PERIOD
00295 0237 39              RTS
00296 0238 97 07   WHEN     STA A   PERIOD
00297 023A 39              RTS
00298 023B 86 FF   BUZZ     LDA A   #$FF
00299 023D 97 05           STA A   BUZTIM    SET BUZZER TIMER.
00300 023F 39              RTS
00301 0240 86 04   CLKSET   LDA A   #4        LOAD STATE DEPENDING IF
00302 0242 7F 0004         CLR     FLAG      H, V, OR T PUSHED.
00303 0245 20 06           BRA     STORE
00304 0247 86 05   VISST    LDA A   #5
00305 0249 20 02           BRA     STORE
00306 024B 86 06   HOMST    LDA A   #6
00307 024D 97 02   STORE    STA A   STATE
00308 024F 39              RTS
00309 0250 96 04   CLOCK    LDA A   FLAG
00310 0252 27 09           BEQ     FINISH
00311 0254 96 09           LDA A   TIME+1    CLOCK DECREMENT ROUTINE.
00312 0256 27 0F           BEQ     PERCY     BRANCH IF TWO LOWEST DIGITS 0
00313 0258 8B 99           ADD A   #$99
00314 025A 19              DAA               DECREMENT 2 LOWEST BITS.
00315 025B 97 09           STA A   TIME+1
00316 025D B6 8003 FINISH  LDA A   PIAAD     RESET IRQ FROM PIA.
00317 0260 3B              RTI
00318 0261 97 04   GONE     STA A   FLAG      CLEAR CLOCK-START FLAG
00319 0263 8D 05           BSR     BUZZ      START BUZZER.
00320 0265 20 F5           BRA     FINISH
00321 0267 96 08   PERCY    LDA A   TIME
00322 0269 27 F5           BEQ     GONE      NO TIME REMAINING.
00323 026B 8B 99           ADD A   #$99      DECREMENT MINUTES.
00324 026D 19              DAA
00325 026E 97 08           STA A   TIME
00326 0270 86 59           LDA A   #$59      SET SECONDS TO 59.
00327 0272 97 09           STA A   TIME+1
00328 0274 20 E6           BRA     FINISH
00329                      END
```